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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,461	MEYER ET AL.	
	Examiner	Art Unit	
	Jae U. Yu	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/16/04 9/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10688461 has a total of 46 claims pending in the application, there are 12 independent claims and 34 dependent claims, all of which are ready for examination by the examiner.

Information Disclosure Statement

As required by M.P.E.P. 609 (C), the applicant's submission of the Information Disclosure Statement dated 8/16/04 and 9/29/05 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 42 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 42 recites the limitation "the communications bus". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claim 15-29, 31-34, 36-40 and 42-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Petersen (WO 95/06285).

2. **Independent claim 15** is a means-plus function claim and interpreted according to 35 USC 112 Sixth paragraph.

"Means ("Local Data Buffer", Page 11) for receiving local data **["Data Unit" n & n-1, Figure 1]** from one or more memory storage units **[Portion of the "System Memory" 12 that corresponds to the "Data Unit n & n-1", Figure 7]" Since the "data unit" is stored (buffered) and shifted in the "Shifter" 1 (Figure 1), the "Shifter" inherently includes the "Local Data Buffer".**

"Means ("Downstream Data Buffer", Page 11) for receiving downstream data over a communications bus **["Data Unit" 1 & 0 (Figure 1) over the bus 16 & 17 (Figure 7)]** from one or more downstream data sources **[Portion of the "System Memory" 12 that corresponds to the "Data Unit 1 & 0", Figure 7]" Since the "data unit" is stored (buffered) and shifted in the "Shifter" 1 (Figure 1), the "Shifter" inherently includes the "Downstream Data Buffer".**

"Means ("Local/Downstream Arbitration Logic Means & Inter-source Arbitration Means") **["Shifter 1 & Control Circuit 2", Figure 1]** for making a determination of how the local data and the downstream data **[Data aligned and sent at one clock cycle, Table 1, Page 11]** will be sent over the communication bus **[Bus 16 and 17, Figure 7]**"

"Allocating one or more first contiguous lanes within a first section of a data block **[Data "22, 21" outputted at the same clock cycle, Line 18, Page 11]** to at least some of the local data, wherein the data block comprises a set of multiple lanes **[Lanes "01(N) – 01(0)", Figure 1]**, and each lane includes a set of configurable bits **[Configurable data outputted, Table 1, Page 11]**"

"Allocating one or more second contiguous lanes within a second section **[Data "24, 23" outputted at the same clock cycle, Line 18, Page 11]** of the data block to at least some of the downstream data, wherein the second section begins at a next lane **[Lanes "01 (3) and 01 (2)", Table 1, Page 11]**, which is contiguous with the first section **[Lanes "01 (1) and 01 (0)", Table 1, Page 11]**"

3. **Claim 16** discloses, "means ("Local Arbitration Means", Page 14) **["System Memory", Figure 7]** for generating a first access request to send the local data over the communications bus **[Sending data "22, 21" to the bus 16 (Figure 7), Page 11 (Table 1)]**".

"Means ("Downstream arbitration logic means", Page 14) **["System Memory", Figure 7]** for generating a second access request to send the downstream data over the communications bus **[Sending the data "24, 23" over the bus 17 (Figure 7), Table 1, Page 11]**"

"Wherein the means for making the determination receives the first access request and the second access request, and bases the determination on the first access request and the second access request **[Table 1 (Page 11) discloses sending the merged data based on the first data and the second data received from the system memory]**"

4. **Claim 17** discloses, "means ("Data Assembly Means", Page 11) **["Shifter 1 & Control Circuit 2", Figure 1]** for arranging the local data and the downstream data into the data block **[Merged data block outputted, Line 18, Page 11]**, according to the determination".

"Means ("Data Assembly Means", Figure 4) for sending the data within the data block over the communications bus **[Sending the merged data block over the bus 16 (Figure 7), Line 18, Page 11]** during a data block transmission period **[Last clock cycle, Line 18, Page 11]**"

5. **Independent claim 18** discloses, "A first circuit **[Input Port "n, n-1", Figure 1]**, which is operable for receiving first source data **[Data "22, 21", Line 17, Page 11]** from a first data source".

"A second circuit **[Input Port "1, 0", Figure 1]**, which is operable for receiving second source data **[Data "24, 23", Line 18, Page 11]** from a second data source"

"A third circuit **[Output Port "0-n", Figure 1]**, which is operable for sending the first source data and the second source data **[Outputting data at one clock cycle, Line 18, Page 11]** over the communications bus **[Bus 16, Figure 7]**"

"Sending the first source data **[Data "22, 21" outputted, Line 18, Page 11]** over the communication bus **[Bus 16, Figure 7]**"

"Identifying a first breakpoint **["01 (1)", Table 1, Page 11]** corresponding to an end of the first source data **[Data "22", Line 18, Page 11]**"

"Sending the second source data **[Outputting Data "23, 24", Line 18, Page 11]** over the communications bus **[Bus 16, Figure 7]** contiguously with the end of the first source data **[Data "22", Line 18, Page 11]**"

"Identifying a second breakpoint **["01 (3)", Table 1, Page 11]** corresponding to an end of the second source data **[Data "24, Line 18, Page 11]**"

6. **Claim 19** discloses, "the first circuit includes a fourth circuit **[Input Port "n, n-1", Figure 1]**, which is operable for receiving downstream data **[Data "22, 21", Line 17, Page 11]** from the communications bus **[Bus 16 & 17, Figure 7]**".

"The second circuit includes a fifth circuit **[Input Port "1, 0", Figure 1]**, which is operable for receiving local data **[Data "24, 23", Line 18, Page 11]** from one or more local memory storage units"

7. **Claim 20** discloses, "arranging a first portion of the first source data within a data block structure **[Data "20, 19" within lanes "01 (3) and 01 (2), Line 17, Page 11]** during a first processing period **[Clock cycle 10, Line 17, Page 11]**, wherein the data block structure includes a fixed number of contiguous, configurable bits **[Contiguous, configurable data outputted, Table 1, Page 11]**".

"Arranging a remainder portion of the first source data within a first section of the data block structure **[Data "22, 21" within lanes "01 (1) and 01 (0)", Line 18, Page 11]** during a second processing period **[Clock cycle 11, Line 18, Page 11]**, wherein the first section includes a first set of contiguous bits **[Configurable data outputted, Table 1, Page 11]**"

8. **Claim 21** discloses, "identifying the first breakpoint **["01 (1)", Line 18, Page 11]** as an end of the first section of the data block structure during the second processing period **[Last transmission cycle, Line 18, Page 11]**".

9. **Claim 22** discloses, "arranging a first portion of the second source data within a second section of the data block **[Data "24, 23" within lanes "01 (3) and 01 (2)", Line 18, Page 11]** during the second processing period **[Clock cycle 11, Line 18, Page 11]**, wherein the second section is contiguous with the first section **[Contiguous with "22 and 21", Line 18, Page 11]**, and the second section includes a second set of contiguous bits **[Contiguous data outputted, Table 1, Page 11]**".

10. **Claim 23** discloses, "the data block structure includes a fixed number of lanes, each lane includes a same number of bits **[1 byte per each lane from 01(0) through 01 (n), Paragraph 1, Page 9]**, the first section of the data block structure includes a first set of the fixed number of lanes **[01 (3) and 01 (2), Line 18, Page 11]**, and the second section of the data block structure includes a second set of the fixed number of lanes **[01 (1) and 01 (0), Line 18, Page 11]**".

11. **Independent claim 24** discloses, "arranging a first portion of first source data within a data block structure **[Data "20, 19" within lanes "01 (3) and 01 (2), Line 17, Page 11]** during a first processing period **[Clock cycle 10, Line 17, Page 11]**, wherein

the data block structure includes a fixed number of contiguous, configurable bits **[Contiguous, configurable data outputted, Table 1, Page 11]**".

"Sending the first portion of the first source data **[Outputting Data "20, 19", Line 17, Page 11]** over the communication bus **[Bus 16, Figure 7]**"

"Arranging a remainder portion of the first source data within a first section of the data block structure **[Data "22, 21" within lanes "01 (1) and 01 (0)", Line 18, Page 11]** during a second processing period **[Clock cycle 11, Line 18, Page 11]**, wherein the first section includes a first set of configurable bits **[Configurable data outputted, Table 1, Page 11]**"

"Arranging a first portion of second source data within a second section of the data block structure **[Data "24, 23" within lanes "01 (3) and 01 (2)", Line 18, Page 11]** during the second processing period **[Clock cycle 11, Line 18, Page 11]**, wherein the second section is contiguous with the first section **[Contiguous with "22 and 21", Line 18, Page 11]**, and the second section includes a second set of contiguous bits **[Contiguous data outputted, Table 1, Page 11]**"

"Sending the remainder portion of the first source data and the first portion of the second source data **[Outputting the merged data, Line 18, Page 11]** over the communications bus **[Bus 16, Figure 7]**"

12. **Claim 25** discloses, "making an indication, during the first processing period **[01 (1) stores 22 during the first clock cycle, Line 17, Page 11]**, that a breakpoint in the first source data will occur during the second processing period".

13. **Claim 26** discloses, "making an indication, during the first processing period **[01 (1) stores 22 during the first clock cycle, Line 17, Page 11]**, of a location of an end of the first section".

14. **Claim 27** discloses, "the data block structure includes a fixed number of lanes **[01 (3) – 01 (0), Table 1, Page 11]**, each lane includes a same number of bits **[1 byte per each lane from 01(0) through 01 (n), Paragraph 1, Page 9]**, the first section of the data block structure includes a first set of the fixed number of lanes **[01 (3) and 01 (2), Line 18, Page 11]**, and the second section of the data block structure includes a second set of the fixed number of lanes **[01 (1) and 01 (0), Line 18, Page 11]**".

15. **Claim 28** discloses, "making an indication, during the first processing period **[01 (1) stores 22 during the first clock cycle, Line 17, Page 11]**, of a lane identifier that corresponds with a last lane of the first section".

16. **Claim 29** discloses, "making an indication, during the first processing period **[01 (2) becomes available for data "23" during the first clock cycle, Line 17, Page 11]**, of a lane identifier that corresponds with a first lane of the second section".

17. **Independent claim 31** discloses, "determining that first source **[Data "22, 21" written, Line 17, Page 11]** and second source data **[Data "24, 23" written, Line 18, Page 11]** are available; allocating one or more first contiguous lanes within a first section of a data block **[Data "22, 21" outputted at the same clock cycle, Line 18, Page 11]** to at least some of the first source data, wherein the data block comprises a set of multiple lanes **[Lanes "01(N) – 01(0)", Figure 1]**, and each lane includes a set of configurable bits **[Configurable data outputted, Table 1, Page 11]**".

"Allocating one or more second contiguous lanes within a second section **[Data "24, 23" outputted at the same clock cycle, Line 18, Page 11]** of the data block to at least some of the second source data, wherein the second section begins at a next lane **[Lanes "01 (3) and 01 (2)", Table 1, Page 11]**, which is contiguous with the first section **[Lanes "01 (1) and 01 (0)", Table 1, Page 11]**"

"Sending, over a communications bus **[Bus 16, Figure 7]** and during a data block transmission period **[Clock cycle 11, Table 11]**, the at least a portion of the first source data within the first section of the data block **[Outputting data "22, 21" within "01 (1) and 01 (0)", Line 18, Page 11**, and the at least a portion of the second source data

within the second section of the data block **[Outputting data "24, 23" within "01 (3) and 01 (2), Line 18, Page 11]**"

18. **Claim 32** discloses, "receiving a first indicator **[Data "21", Table 1, Page 11]** that the first source data is available from a first data source".

"Receiving a second indicator **[Data "24", Table 1, Page 11]** that the second source data is available from a second data source"

19. **Claim 33** discloses, "receiving a first request **[Data "21", Table 1, Page 11]** to send the first source data over the communication bus".

"Receiving a second request **[Data "24", Table 1, Page 11]** to send the second source data over the communication bus"

20. **Claim 34** discloses, "Receiving information that enables an identification of which lane is the next, contiguous lane **[Lane 01 (1) is contiguous with lane 01 (2), Table 1, Page 11]**".

"Allocating a number of lanes to the at least some of the second source data **[Data "24 and 23" in lanes 01 (2) and 01 (3), Line 18, Page 11]**, wherein a first lane of the

number of lanes is the next, contiguous lane **[Contiguous with lanes 01 (1) and 01 (0), Table 1, Page 11]**"

21. **Independent claim 36** disclose, "arranging first source data from a first source within a first section of a data block structure **[Data "22, 21" within lanes "01 (1) and 01 (0)", Line 18, Page 11]**, wherein the data block structure includes a fixed number of contiguous, configurable bits **["01 (1)", Table 1, Page 11]**, and data within the data block structure is periodically sent out **[Outputting data during each clock cycle, Table 1, Page 11]** on a communication bus **[Bus 16, Figure 7]**".

"Determining that second source data **[Data "24, 23" available for transmission, Table 1, Page 11]** from a second source is available to be sent over the communication bus **[Bus 16, Figure 7]**"

"Requesting access **[Outputting data "24, 23", Line 18, Page 11]** to the communication bus **[Bus 16, Figure 7]** to send the second source data"

"Receiving an indication of where, within the data block structure, at least a portion of the second source data should be placed **[The second source data should be placed after "01 (1)" which corresponds to an end of the first source data, Table 1, Page 11]**"

"Arranging the at least a portion of the second source data within the data block structure according to the indication **[Data "24, 23" arranged after "01 (1)", Line 18, Page 11]**, resulting in the at least a portion of the second source data occupying a second section of the data block that is contiguous with an end of the first section **[Data "24, 23" is contiguous with data "22", Line 18, Page 11]**"

"Sending the first source data and the at least a portion of the second source data over the communications bus **[Outputting the merged data over the bus 16 (Figure 7), Line 18, Page 11]** during a data block transmission period **[Transmission clock cycle, Table 1, Page 11]**"

22. **Claim 37** discloses, "the data block structure includes a fixed number of lanes **[01 (3) – 01 (0), Table 1, Page 11]**, each lane includes a same number of bits **[1 byte per each lane from 01(0) through 01 (n), Paragraph 1, Page 9]**, the first section of the data block structure includes a first set of the fixed number of lanes **[01 (3) and 01 (2), Line 18, Page 11]**, and the second section of the data block structure includes a second set of the fixed number of lanes **[01 (1) and 01 (0), Line 18, Page 11]**".

23. **Claim 38** discloses, "receiving lane identifier **["01 (1)" corresponding to data "22", Line 18, Page 11]** that corresponds with a last lane of the first section".

24. **Claim 39** discloses, "receiving a lane identifier **["01 (2)" corresponding to data "23", Line 18, Page 11]** that corresponds with a first lane of the second section".

25. **Claim 40** discloses, "predicting where a breakpoint will occur in the second source data". **The end of the first source data "22" at lane "01 (1)" inherently predicts that the second source data breakpoint will occur at lane "01 (2)".**

26. **Independent claim 42** discloses, "arranging first source data within a first section of a data block structure **[Data "22, 21", Line 18, Page 11]**, wherein the data block structure includes fixed number of contiguous, configurable bits **["01 (1)", Table 1, Page 11]**".

"Receiving a request to send second source data over **[Outputting data "24, 23", Line 18, Page 11]** the communication bus **[Bus 16, Figure 7]**"

"Identifying a location of a breakpoint in the first source data **["01 (1), Table 1, Page 11]**"

"Arranging at least a portion of the second source data within a second section of the data block structure after the breakpoint **[Arranging "24, 23" after "01 (1)", Line 18, Page 11]**, wherein the second section is contiguous with an end of the first section **[Data "24, 23" contiguous with "22", Line 18, Page 11]**"

"Sending the first source data and the at least a portion of the second source data over the communications bus **[Outputting the merged data over the bus 16 (Figure 7), Line 18, Page 11]** during a data block transmission period **[Transmission clock cycles, Table 1, Page 11]**"

27. **Claim 43** discloses, "the data block structure includes a fixed number of lanes **[01 (3) – 01 (0), Table 1, Page 11]**, each lane includes a same number of bits **[1 byte per each lane from 01(0) through 01 (n), Paragraph 1, Page 9]**, the first section of the data block structure includes a first set of the fixed number of lanes **[01 (3) and 01 (2), Line 18, Page 11]**, and the second section of the data block structure includes a second set of the fixed number of lanes **[01 (1) and 01 (0), Line 18, Page 11]**".

28. **Claim 44** discloses, "receiving lane identifier **["01 (1)" corresponding to data "22", Line 18, Page 11]** that corresponds with a last lane of the first section".

29. **Claim 45** discloses, "receiving a lane identifier **["01 (2)" corresponding to data "23", Line 18, Page 11]** that corresponds with a first lane of the second section".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-8 and 12-14 are rejected under 35 USC 103 (a) as being obvious over Gallagher et al. (US 5,809,253) in view of Petersen (WO 95/06285).

2. As per **independent claims 1 and 7**, Gallagher et al. disclose, "a processor **["Management Agent Module" 610, Figure 3]**, which generates and sends one or more memory access requests".

"Multiple memory modules **["Line Card 1 & 2", Figure 3]**, operatively coupled together through a communications bus **[Coupled together through the "Management Agent Module" 610, Figure 3]**, which returns data requested in the one or more memory access requests, wherein each of the multiple memory module is a data source"

"One or more memory storage units **["Memory" 645, Figure 3]** for storing local data"

Petersen discloses, "a hub **["Peripheral Device" 15, Figure 7]**, operatively coupled to the one or more memory storage units **["System Memory" 12, Figure 7]** and to a communications bus **[Bus 16, Figure 7]** over which the hub can receive downstream data from one or more other hubs".

"Determining that first source data and second source data are available **["Data "22, 21" and "24, 23" are available for transmission, Table 1, Page 11]**"

"Allocating one or more first contiguous lane within a first section of a data block **[Data "22, 21" outputted at the same clock cycle, Line 18, Page 11]** to at least some of the first source data, wherein the data block comprises a set of multiple lanes **[Lanes "01(N) – 01(0)", Figure 1]**, and each lane includes a set of configurable bits **[Configurable data outputted, Table 1, Page 11]**"

"Allocating one or more second contiguous lanes within a second section **[Data "24, 23" outputted at the same clock cycle, Line 18, Page 11]** of the data block to at least some of the second source data, wherein the second section begins at a next lane **[Lanes "01 (3) and 01 (2)", Table 1, Page 11]**, which is contiguous with the first section **[Lanes "01 (1) and 01 (0)", Table 1, Page 11]**"

"Sending, over a communications bus **[Bus 16, Figure 7]** and during a data block transmission period **[Clock cycle 11, Table 11]**, the at least a portion of the first source data within the first section of the data block **[Outputting data "22, 21" within "01 (1) and 01 (0)", Line 18, Page 11**, and the at least a portion of the second source data within the second section of the data block **[Outputting data "24, 23" within "01 (3) and 01 (2), Line 18, Page 11]**"

Gallagher et al. and Petersen are analogous art because they are from the same field of endeavor of data transferring.

At the time of the invention it would have been obvious to modify Gallagher et al. by including a hub that performs the data merging operation as taught by Petersen in Figure 1 and 7.

The motivation for doing so would have been efficiently transferring segments of data of arbitrary width and alignment as expressly taught by Petersen at lines 6-11, on page 6.

Therefore, it would have been obvious to combine Petersen with Gallagher et al. for the benefit of efficient data transfer to obtain the invention as specified in claims 1 and 7.

3. Claim 2 discloses, "a link controller **["Management Agent Module" 610, Figure 3, Gallagher et al.]**, operatively coupled between the processor **["Host Processor", Figure 7, Petersen]** and at least one of the multiple memory modules **["Line Card", Figure 3]**, which is operable for receiving the one or more memory access requests, and generating and sending one or more memory access commands **[Abstract, Gallagher et al.]**, based on the one or more memory access requests, to the multiple memory modules over the communication bus".

4. Claim 3 discloses, "the communications bus **[Bus 16, Figure 7]".**

"Receiving data from one or more other memory modules **[Line Cards, Figure 3, Gallagher et al.]** from a downstream direction on a first part of the communications bus **[Bus 17, Figure 7, Petersen]**"

"Sending the at least a portion of the first source data and the at least a portion of the second source data toward the link controller **["Management Agent Module" 610, Figure 3, Gallagher et al.]** on a second part of the communication bus **[Bus 16, Figure 7, Petersen]**"

5. **Claim 4 and 13** discloses, "a first circuit **[Input ports "n, n-1", Figure 1, Petersen]**, which is operable for receiving downstream data from a second memory module **[Line Cards, Figure 3, Gallagher et al.]** over the communication bus **[Bus 17, Figure 7, Petersen]**, wherein the downstream data is the first source data".

"A second circuit **[Input ports "1, 0", Figure 1, Petersen]** which is operable for receiving local data from one or more memory storage units **["System Memory", Figure 7, Petersen]** accessible to the memory module"

"A third circuit **["Data Aligner", Figure 7, Petersen]**, which is operable for assembling the downstream data and the local data into the data block **[Data block assembled, Table 1, Page 11]**"

6. **Claim 5 and 14** disclose, "a first circuit **[Input ports "1, 0", Figure 1, Petersen]** which is operable for receiving local data from one or more memory storage units **["System Memory", Figure 7, Petersen]** accessible to the memory module"

"A second circuit **[Input ports "n, n-1", Figure 1, Petersen]**, which is operable for receiving downstream data from a second memory module **[Line Cards, Figure 3, Gallagher et al.]** over the communication bus **[Bus 17, Figure 7, Petersen]**".

"A third circuit **["Data Aligner", Figure 7, Petersen]**, which is operable for assembling the downstream data and the local data into the data block **[Data block assembled, Table 1, Page 11]**"

7. **Claim 6** discloses, "the electronic system is a computer **[Figure 7, Petersen]**".

8. **Claim 8** discloses, "memory storage units and the hub are co-located on a single substrate **["Line Cards", Figure 3, Gallagher et al.]** that is irremovably connectable to the communication bus **[Column 7, Lines 54-60]**".

9. **Claim 12** discloses, "application specific integrated circuits **[Implemented in ASIC, Column 7, Lines 49-51]**".

10. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al. (US 5,809,253) and Petersen (WO 95/06285) as applied to claim 7 above, and further in view of Friedman et al. (US 2002/0167829).

11. As per **claim 9 and 10**, Petersen and Gallagher et al. disclose the apparatus recited in claim 7.

Petersen and Gallagher et al. do not disclose expressly, "the one or more memory storage units includes one or more dynamic random access memory components".

Friedman et al. disclose, "DRAM cells" in paragraph 36.

Petersen, Gallagher et al. and Friedman et al. are analogous art because they are from the same field of endeavor of data control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Petersen and Gallagher et al. by including "DRAM cells" as taught by Friedman et al. in paragraph 36.

The motivation for doing so would have been "a dense and relatively fast memory" as expressly taught by Friedman et al. in paragraph 36.

Therefore, it would have been obvious to combine Friedman et al. with Petersen and Gallagher et al. for the benefit of fast and dense storage device to obtain the invention as specified in claims 9 and 10.

12. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al. (US 5,809,253) and Petersen (WO 95/06285) as applied to claim 7 above, and further in view of Dancs et al. (US 2001/0016877).

13. As per **claim 11**, Petersen and Gallagher et al. disclose the apparatus recited in claim 7.

Petersen and Gallagher et al. do not disclose expressly, "read only memory".

Dancs et al. disclose, "ROM" in paragraph 53.

Petersen, Gallagher et al. and Dancs et al. are analogous art because they are from the same field of endeavor of data control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Petersen and Gallagher et al. by including "ROM" as taught by Dancs et al. in paragraph 53.

The motivation for doing so would have been to "guarantee data integrity" as expressly taught by Dancs et al. in paragraph 53.

Therefore, it would have been obvious to combine Dancs et al. with Petersen and Gallagher et al. for the benefit of data integrity to obtain the invention as specified in claim 11.

14 Claim 30, 35, 41 and 46 are rejected under 35 USC 103 (a) as being obvious over Petersen (WO 95/06285) in view of Zwern (US 2001/0035845).

15. As per **independent claim 30**, Petersen discloses:

"Arranging a first portion of first source data within a data block structure **[Data "20, 19" within lanes "01 (3) and 01 (2), Line 17, Page 11]** during a first processing period **[Clock cycle 10, Line 17, Page 11]**, wherein the data block structure includes a fixed number of contiguous, configurable bits **[Contiguous, configurable data outputted, Table 1, Page 11]**".

"Sending the first portion of the first source data **[Outputting Data "20, 19", Line 17, Page 11]** over the communication bus **[Bus 16, Figure 7]**"

"Arranging a remainder portion of the first source data within a first section of the data block structure **[Data "22, 21" within lanes "01 (1) and 01 (0)", Line 18, Page 11]**

during a second processing period **[Clock cycle 11, Line 18, Page 11]**, wherein the first section includes a first set of configurable bits **[Configurable data outputted, Table 1, Page 11]**"

"Arranging a first portion of second source data within a second section of the data block structure **[Data "24, 23" within lanes "01 (3) and 01 (2)", Line 18, Page 11]** during the second processing period **[Clock cycle 11, Line 18, Page 11]**, wherein the second section is contiguous with the first section **[Contiguous with "22 and 21", Line 18, Page 11]**, and the second section includes a second set of contiguous bits **[Contiguous data outputted, Table 1, Page 11]**"

"Sending the remainder portion of the first source data and the first portion of the second source data **[Outputting the merged data, Line 18, Page 11]** over the communications bus **[Bus 16, Figure 7]**"

Petersen does not disclose expressly, "a computer-readable medium having a computer-executable instructions".

Zwern discloses, "a custom software module" in paragraph 80, wherein the "software module" corresponds to the "computer executable instructions" from the claim. Since the "software module" is a substitute for the "hardware"

(Paragraph 80), the "software" is inherently stored in a computer readable medium and executed in a computer system.

Petersen and Zwern are analogous art because they are from the same field of endeavor of computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Petersen by implementing Petersen's transmission method in the form of "software module" as taught by Zwern in paragraph 80.

The motivation for doing so would have been to "avoid hardware costs, while providing the greatest flexibility" as expressly taught by Zwern in paragraph 80.

Therefore, it would have been obvious to combine Zwern with Petersen for the benefit of low cost and high flexibility to obtain the invention as specified in claim 30.

16. As per **independent claim 35**, Petersen discloses:

"Determining that first source **[Data "22, 21" written, Line 17, Page 11]** and second source data **[Data "24, 23" written, Line 18, Page 11]** are available; allocating one or more first contiguous lanes within a first section of a data block **[Data "22, 21" outputted at the same clock cycle, Line 18, Page 11]** to at least some of the first source data, wherein the data block comprises a set of multiple lanes **[Lanes "01(N) – 01(0)", Figure 1]**, and each lane includes a set of configurable bits **[Configurable data outputted, Table 1, Page 11]**".

"Allocating one or more second contiguous lanes within a second section **[Data "24, 23" outputted at the same clock cycle, Line 18, Page 11]** of the data block to at least some of the second source data, wherein the second section begins at a next lane **[Lanes "01 (3) and 01 (2)", Table 1, Page 11]**, which is contiguous with the first section **[Lanes "01 (1) and 01 (0)", Table 1, Page 11]**"

"Sending, over a communications bus **[Bus 16, Figure 7]** and during a data block transmission period **[Clock cycle 11, Table 11]**, the at least a portion of the first source data within the first section of the data block **[Outputting data "22, 21" within "01 (1) and 01 (0)", Line 18, Page 11**, and the at least a portion of the second source data within the second section of the data block **[Outputting data "24, 23" within "01 (3) and 01 (2), Line 18, Page 11]**"

Petersen does not disclose expressly, "a computer-readable medium having a computer-executable instructions".

Zwern discloses, "a custom software module" in paragraph 80, wherein the "software module" corresponds to the "computer executable instructions" from the claim. Since the "software module" is a substitute for the "hardware" (Paragraph 80), the "software" is inherently stored in a computer readable medium and executed in a computer system.

Petersen and Zwern are analogous art because they are from the same field of endeavor of computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Petersen by implementing Petersen's transmission method in the form of "software module" as taught by Zwern in paragraph 80.

The motivation for doing so would have been to "avoid hardware costs, while providing the greatest flexibility" as expressly taught by Zwern in paragraph 80.

Therefore, it would have been obvious to combine Zwern with Petersen for the benefit of low cost and high flexibility to obtain the invention as specified in claim 35.

17. As per **independent claim 41**, Petersen discloses:

"Arranging first source data from a first source within a first section of a data block structure **[Data "22, 21" within lanes "01 (1) and 01 (0)", Line 18, Page 11]**, wherein the data block structure includes a fixed number of contiguous, configurable bits **["01 (1)", Table 1, Page 11]**, and data within the data block structure is periodically sent out **[Outputting data during each clock cycle, Table 1, Page 11]** on a communication bus **[Bus 16, Figure 7]**".

"Determining that second source data **[Data "24, 23" available for transmission, Table 1, Page 11]** from a second source is available to be sent over the communication bus **[Bus 16, Figure 7]**"

"Requesting access **[Outputting data "24, 23", Line 18, Page 11]** to the communication bus **[Bus 16, Figure 7]** to send the second source data"

"Receiving an indication of where, within the data block structure, at least a portion of the second source data should be placed **[The second source data should be placed after "01 (1)" which corresponds to an end of the first source data, Table 1, Page 11]**"

"Arranging the at least a portion of the second source data within the data block structure according to the indication **[Data "24, 23" arranged after "01 (1)", Line 18, Page 11]**, resulting in the at least a portion of the second source data occupying a second section of the data block that is contiguous with an end of the first section **[Data "24, 23" is contiguous with data "22", Line 18, Page 11]**"

"Sending the first source data and the at least a portion of the second source data over the communications bus **[Outputting the merged data over the bus 16 (Figure 7), Line 18, Page 11]** during a data block transmission period **[Transmission clock cycle, Table 1, Page 11]**"

Petersen does not disclose expressly, "a computer-readable medium having a computer-executable instructions".

Zwern discloses, "a custom software module" in paragraph 80, wherein the "software module" corresponds to the "computer executable instructions" from the claim. Since the "software module" is a substitute for the "hardware" (Paragraph 80), the "software" is inherently stored in a computer readable medium and executed in a computer system.

Petersen and Zwern are analogous art because they are from the same field of endeavor of computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Petersen by implementing Petersen's transmission method in the form of "software module" as taught by Zwern in paragraph 80.

The motivation for doing so would have been to "avoid hardware costs, while providing the greatest flexibility" as expressly taught by Zwern in paragraph 80.

Therefore, it would have been obvious to combine Zwern with Petersen for the benefit of low cost and high flexibility to obtain the invention as specified in claim 41.

18. As per **independent claim 46**, Petersen discloses:

"Arranging first source data within a first section of a data block structure **[Data "22, 21", Line 18, Page 11]**, wherein the data block structure includes fixed number of contiguous, configurable bits **["01 (1)", Table 1, Page 11]**".

"Receiving a request to send second source data over **[Outputting data "24, 23", Line 18, Page 11]** the communication bus **[Bus 16, Figure 7]**"

"Identifying a location of a breakpoint in the first source data **["01 (1), Table 1, Page 11]**"

"Arranging at least a portion of the second source data within a second section of the data block structure after the breakpoint **[Arranging "24, 23" after "01 (1)", Line 18, Page 11]**, wherein the second section is contiguous with an end of the first section **[Data "24, 23" contiguous with "22", Line 18, Page 11]**"

"Sending the first source data and the at least a portion of the second source data over the communications bus **[Outputting the merged data over the bus 16 (Figure 7), Line 18, Page 11]** during a data block transmission period **[Transmission clock cycles, Table 1, Page 11]**"

Petersen does not disclose expressly, "a computer-readable medium having a computer-executable instructions".

Zwern discloses, "a custom software module" in paragraph 80, wherein the "software module" corresponds to the "computer executable instructions" from the claim. Since the "software module" is a substitute for the "hardware" (Paragraph 80), the "software" is inherently stored in a computer readable medium and executed in a computer system.

Petersen and Zwern are analogous art because they are from the same field of endeavor of computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Petersen by implementing Petersen's transmission method in the form of "software module" as taught by Zwern in paragraph 80.

The motivation for doing so would have been to "avoid hardware costs, while providing the greatest flexibility" as expressly taught by Zwern in paragraph 80.

Therefore, it would have been obvious to combine Zwern with Petersen for the benefit of low cost and high flexibility to obtain the invention as specified in claim 46.

Relevant Art Cited by the Examiner

Non-patent Literature	**Figures**
"IEE Std 1596.4-1996 – IEEE Standard for High-Bandwidth Memory Interface Based on Scalable Coherent Interface (SCI) Signaling	2

Technology (RamLink)" 12/31/1996.

Conclusion

A. Claims Rejected in the Application

Per the instant office action, claims 1-46 have received a first action on the merits and are subject of a first action non-final.

B. Direction of Future Correspondences

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae U. Yu whose telephone number is 571-272-1133. The examiner can normally be reached on M-F 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 2, 2006

Jae Un Yu
Art Unit 2185

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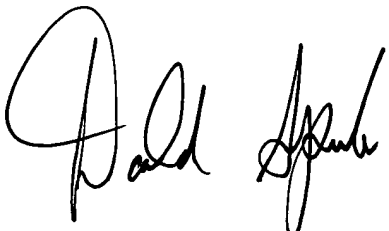

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